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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
35997-217836

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Application Number	Filed
09/932,408	August 18, 2001

First Named Inventor: Russell Dickerson et al.

Art Unit	Examiner
2131	Longbit Chai

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record. Registration number 47,294

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Edward W. Yee
Signature

Edward W. Yee
Typed or printed name

202-344-4632
Telephone number

OCT. 11, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

Docket No.: 35997-217836
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Dickerson et al.

Application No.: 09/932,408 | Confirmation No.: 4316

Filed: August 18, 2001 | Art Unit: 2131

For: METHOD AND SYSTEM FOR MAINTAINING SECURE SEMICONDUCTOR DEVICE AREAS | Examiner: L. Chai

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MAIL STOP AFTER FINAL
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated May 10, 2005 finally rejecting claims 1-24 and the Advisory Action dated August 24, 2005, Applicants submit the following remarks.

REMARKS

Reconsideration of this Application is respectfully requested.

Rejections under 35 U.S.C. § 103

On pages 11-16, the Final Office Action (hereinafter "Action") rejects claims 2, 4, 5, 10, 11, 17, and 18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,088,262 to Nasu (hereinafter Nasu) in view of U.S. Patent Application Publication No. 2003/0212897, which is the publication of the instant application. The Action refers to the Publication as "AAP," which will be

used in this response for consistency. Applicants note that the Action also appears to reject claim 24 as being obvious over Nasu in view of AAP (see Action, pages 11-13) even though claim 24 is not listed as being rejected in section 11 on page 11 of the Action.

Applicants respectfully traverse the rejection as the Action fails to establish a *prima facie* case of obviousness.

On pages 11-13, the Action rejects claim 24. Claim 24 recites: "A system for obstructing access to a secure area of a semiconductor device comprising: a microprocessor core; a decoder connected to an output of the microprocessor core; a control line connected to an output of the decoder; a circuit for supplying output data; a data output line connected to an output of the circuit for supplying output data; and an AND gate having a first input connected to the control line, a second input connected to the data output line, and an output connected to an input of a buffer; and a port implemented in the semiconductor device for connecting to an in-circuit emulator, wherein a line on the port is also connected to an output of the buffer, wherein **when** the in-circuit emulator **requests access** to the secure area, the microprocessor core generates microprocessor signals for decoding by the decoder, and wherein the decoder decodes the microprocessor signals and generates a control signal on the control line connected to the first input of the AND gate, and wherein the AND gate outputs an obstructing signal to **obstruct access** by the in-circuit emulator to **the secure area**." (Emphasis added.)

For at least the following reasons, the combined teachings of Nasu and AAP do not teach or suggest all of the claim features to render claim 24 obvious under 35 U.S.C. § 103(a).

Neither Nasu nor AAP teach the sequence of events that occur when an in-circuit emulator requests access to a secure area to obstruct access to the secure area, as recited by the claimed invention. Specifically, Nasu and AAP do not teach or suggest "wherein **when** the in-circuit emulator **requests access to the secure area**, the microprocessor core generates microprocessor signals for decoding by the decoder, and wherein the decoder decodes the microprocessor signals and generates a control signal on the control line connected to the first input of the AND gate, and wherein the AND gate outputs an obstructing signal to **obstruct access** by the in-circuit emulator **to the secure area**," (emphasis added) as recited in claim 24.

The Action relies on paragraph [0030] of AAP and column 1, lines 55-57 of Nasu as teaching these features. The following will first consider the teachings of AAP, and then the teachings of Nasu. In paragraph [0030], AAP describes the components of semiconductor device 20 depicted in FIG. 3A. AAP teaches that the semiconductor device 20 may include microprocessor core 40, supervisor mode memory 44, and support or glue logic 46 connected to control line 50. AAP also teaches that the support logic 46 may include a decoder and that an in-circuit emulator (ICE) 10 may read and write to the semiconductor device 20 through port 22 (se AAP paragraph [0028]). AAP teaches the protected secure areas are the supervisor mode memory 44 and secure registers (see AAP, paragraph [0030]). On page 12, the Action equates the claimed "microprocessor core," "decoder," "control line," and "in-circuit emulator" with the microprocessor core 40, the support or glue logic 46, the control line 50, and the ICE 10 of AAP, respectively.

However, AAP does not teach or suggest a sequence of events that occurs **when** an in-circuit emulator **requests access** to a secure area that leads to the output of an obstruction signal to **obstruct access** by the in-circuit emulator **to the secure area**, as recited in claim 24.. Particularly, AAP does not teach or suggest the ICE 10 requesting access to the supervisor mode memory 44. AAP also does not teach that **when** the ICE 10 **requests access** to the supervisor mode memory 44, the microprocessor core 40 generates microprocessor signals for decoding by the decoder of the support logic 46. Lastly, AAP does not teach that the decoder decodes the microprocessor signals and generates a control signal on the control line 50 that **obstructs access** by the ICE 10 to the supervisor mode memory 44.

Instead, AAP teaches that if a user issues a software interrupt (SWI) to direct the microprocessor core 40 to change into a supervisor mode, the secure areas of the semiconductor device 20, such as the supervisor mode memory 44, may be available to the user at port 22, completely defeating the purpose of a secure mode (see AAP, paragraph [0030]). Nowhere does AAP teach that the ICE 10 requests access to the supervisory mode memory 44, and AAP also does not teach the microprocessor core 40 generating signals that are used by other devices to obstruct access by the ICE 10 to the supervisory mode memory 44. Hence, AAP does not teach or suggest that when the ICE 10 requests access to the supervisory mode memory 44, the microprocessor core 40 generates microprocessor signals for decoding by the decoder of the support logic 46, and AAP

also does not teach that the decoder decodes the microprocessor and generates a control signal on the control line 50 to obstruct access by the ICE 10 to the supervisory mode memory 44. Thus, AAP does not teach or suggest "wherein **when** the in-circuit emulator **requests access** to the secure area, the microprocessor core generates microprocessor signals for decoding by the decoder, and wherein the decoder decodes the microprocessor signals and generates a control signal on the control line connected to the first input of the AND gate, and wherein the AND gate outputs an obstructing signal to **obstruct access** by the in-circuit emulator **to the secure area**," (emphasis added) as recited in claim 24.

Referring now to the teachings of Nasu, similar to AAP, Nasu does not teach or suggest a sequence of events that occurs **when** an in-circuit emulator requests access to a secure area that obstructs access by the in-circuit emulator to the secure area, as recited in claim 24. On page 13, the Action cites the read protection means described in column 1, lines 55-57 as teaching the claim features. Applicants respectfully disagree.

Nasu also fails to teach any similar sequence of events performed by the read protection means as that recited in claim 24. The read protection means of Nasu is further described in column 5, line 5-column 6, line 14. In this section, Nasu teaches a read protection control circuit 107 that may be used to prevent data from being written into or read from a memory cell array 100. Nasu teaches that the read protection control circuit 107 sets the read protection for the memory cell array 100 using the read protection setting signal 117 (see Nasu, col. 5, lines 63-67, also see col. 5, lines 5-18). Nasu teaches that the read protection is set **after** the user of the microcomputer has developed a program and written that program into memory cell array 100 to protect the written program from being copied by third parties (see Nasu, col. 5, line 63-col. 6, line 1).

However, Nasu does not teach or suggest that **when** a third party requests access to the memory cell array 100, the read protection control circuit 107 (or along with other devices) generates a read protection setting signal 117 to obstruct access by the third party to the memory cell array 100." Thus, Nasu does not teach or suggest "wherein **when** the in-circuit emulator **requests access** to the secure area, the microprocessor core generates microprocessor signals for decoding by the decoder, and wherein the decoder decodes the microprocessor signals and generates a control signal on the control line connected to the first input of the AND gate, and wherein the

AND gate outputs an obstructing signal to **obstruct access** by the in-circuit emulator **to the secure area**," (emphasis added) as recited in claim 24. Therefore, the combined teachings of AAP and Nasu do not teach a similar sequence of events occurring **when** an in-circuit emulator **requests access** to a secure area to obstruct access by the in-circuit emulator to the secure area and do not render claim 24 obvious under 35 U.S.C. § 103(a).

Accordingly, claim 24 is allowable over the combined teachings of Nasu and AAP and allowance thereof is respectfully requested.

Conclusion

Applicants submit at least one clear error exists in the final rejection mailed May 10, 2005 by the omission of elements cited in claim 24 required to establish *prima facie* case of obviousness under 35 U.S.C. § 103(a). Applicants also request entry of the amendment filed August 10, 2005 and believe that this amendment places claims 1-9, 11-16, and 19-23 in condition for allowance for reasons analogous to those give in support of claim 24.

Respectfully submitted,

Dated: OCT. 11, 2005

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